

Notice of Allowability

Application No.

10/671,339

Examiner

Y. J. Han

Applicant(s)

KAWAGUCHI ET AL.

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to an IDS filed on 9/25/03.
2. ☒ The allowed claim(s) is/are 1-20.
3. ☒ The drawings filed on 25 September 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 9/25/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


JESSICA HAN
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-20 are allowed.
2. The following is an examiner's statement of reasons for allowance: ✓

Claim 1 recites, inter alia, at least one of first and second transistors provided in the semiconductor device, the first transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the output terminal of the voltage generating circuit and a gate supplied with constant voltage and having negative threshold voltage and the second transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the output terminal of the reference voltage generating circuit and a gate supplied with constant voltage and having negative threshold voltage.

Claim 4 recites, inter alia, a first transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the output terminal of the voltage generating circuit and a gate supplied with first voltage and having negative threshold voltage; and at least one of second and third transistors provided in the semiconductor device, the second transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the first output terminal of the reference voltage generating circuit and a gate supplied with second voltage and having negative threshold voltage and the third transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the second output terminal of the reference voltage generating circuit and a gate supplied with preset voltage and having negative threshold voltage.

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Claim 14 recites, inter alia, a transistor having a current path connected at one end to a terminal to which the external power supply voltage is supplied and connected at the other end to one of the output terminal of the voltage generating circuit and the output terminal of the reference voltage generating circuit, the transistor being supplied with constant voltage at a gate thereof and having negative threshold voltage.

Claim 16 recites, inter alia, a first transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the output terminal of the voltage generating circuit and a gate supplied with first voltage and having negative threshold voltage; and a second transistor having a current path connected between a terminal to which the external power supply voltage is supplied and the second output terminal of the reference voltage generating circuit and having negative threshold voltage, a gate of the second transistor being grounded.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include either of the above limitations.

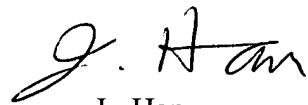
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Y. J. Han whose telephone number is 571-272-2078. The examiner can normally be reached on Mon-Fri 5:30am-2:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



J. Han
Primary Examiner
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